NEC

Customer Notification

V850ES/Fx3

32-Bit Single-Chip Microcontroller

Operating Precautions

V850ES/FE3:
µPD70F3370A
µPD70F3371

V850ES/FF3:
µPD70F3372
µPD70F3373

V850ES/FG3:
µPD70F3374
µPD70F3375
µPD70F3376A
µPD70F3377A

V850ES/FJ3:
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µPD70F3379
µPD70F3380
µPD70F3381
µPD70F3382

V850ES/FK3:
µPD70F3383
µPD70F3384
µPD70F3385

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(A) Table of Operating Precautions

V850ES/FE3

Outline			μPD70F3370A
		Rev.	
		Rank[a]	
No. 1	Boot Cluster Swapping (I) (Direction of usage)		×
No. 2	Boot Cluster Swapping (II) (Direction of usage)		×
No. 3	Interrupt handling during self-programming mode (Specification change notice)		✓
No. 4	Subclock selection for WT, TAA, TMM (Specification change notice)		×
No. 5	TAA, TAB Anytime write delay (Direction of use)		×
No. 6	Code Flash and Data Flash operation (Specification Change Notice)		×

a. The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

Outline			μPD70F3371
		Rev.	
		Rank[a]	
No. 1	Boot Cluster Swapping (I) (Direction of usage)		×
No. 2	Boot Cluster Swapping (II) (Direction of usage)		×
No. 3	Interrupt handling during self-programming mode (Specification change notice)		✓
No. 4	Subclock selection for WT, TAA, TMM (Specification change notice)		×
No. 5	TAA, TAB Anytime write delay (Direction of use)		×
No. 6	Code Flash and Data Flash operation (Specification Change Notice)		×

a. The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

✓: Not applicable
×: Applicable

V850ES/FF3

Outline			μPD70F3372
		Rev.	
		Rank[a]	
No. 1	Boot Cluster Swapping (I) (Direction of usage)		×
No. 2	Boot Cluster Swapping (II) (Direction of usage)		×
No. 3	Interrupt handling during self-programming mode (Specification change notice)		✓
No. 4	Subclock selection for WT, TAA, TMM (Specification change notice)		×
No. 5	TAA, TAB Anytime write delay (Direction of use)		×
No. 6	Code Flash and Data Flash operation (Specification Change Notice)		×

a. The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

Outline			μPD70F3373
		Rev.	
		Rank[a]	
No. 1	Boot Cluster Swapping (I) (Direction of usage)		×
No. 2	Boot Cluster Swapping (II) (Direction of usage)		×
No. 3	Interrupt handling during self-programming mode (Specification change notice)		✓
No. 4	Subclock selection for WT, TAA, TMM (Specification change notice)		×
No. 5	TAA, TAB Anytime write delay (Direction of use)		×
No. 6	Code Flash and Data Flash operation (Specification Change Notice)		×

a. The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

✓: Not applicable
×: Applicable

V850ES/FG3

Outline			μPD70F3374
		Rev.	
		Rank[a]	
No. 1	Boot Cluster Swapping (I) (Direction of usage)		×
No. 2	Boot Cluster Swapping (II) (Direction of usage)		×
No. 3	Interrupt handling during self-programming mode (Specification change notice)		✓
No. 4	Subclock selection for WT, TAA, TMM (Specification change notice)		×
No. 5	TAA, TAB Anytime write delay (Direction of use)		×
No. 6	Code Flash and Data Flash operation (Specification Change Notice)		×

a. The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

Outline			μPD70F3375
		Rev.	
		Rank[a]	
No. 1	Boot Cluster Swapping (I) (Direction of usage)		×
No. 2	Boot Cluster Swapping (II) (Direction of usage)		×
No. 3	Interrupt handling during self-programming mode (Specification change notice)		✓
No. 4	Subclock selection for WT, TAA, TMM (Specification change notice)		×
No. 5	TAA, TAB Anytime write delay (Direction of use)		×
No. 6	Code Flash and Data Flash operation (Specification Change Notice)		×

a. The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

Outline			µPD70F3376A
		Rev.	
		Rank[a]	
No. 1	Boot Cluster Swapping (I) (Direction of usage)		✓
No. 2	Boot Cluster Swapping (II) (Direction of usage)		✓
No. 3	Interrupt handling during self-programming mode (Specification change notice)		✓
No. 4	Subclock selection for WT, TAA, TMM (Specification change notice)		×
No. 5	TAA, TAB Anytime write delay (Direction of use)		×
No. 6	Code Flash and Data Flash operation (Specification Change Notice)		×

a. The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

Outline			µPD70F3377A
		Rev.	
		Rank[a]	
No. 1	Boot Cluster Swapping (I) (Direction of usage)		✓
No. 2	Boot Cluster Swapping (II) (Direction of usage)		✓
No. 3	Interrupt handling during self-programming mode (Specification change notice)		✓
No. 4	Subclock selection for WT, TAA, TMM (Specification change notice)		×
No. 5	TAA, TAB Anytime write delay (Direction of use)		×
No. 6	Code Flash and Data Flash operation (Specification Change Notice)		×

a. The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

✓: Not applicable
×: Applicable

V850ES/FJ3

Outline			μPD70F3378
		Rev.	
		Rank[a]	
No. 1	Boot Cluster Swapping (I) (Direction of usage)		×
No. 2	Boot Cluster Swapping (II) (Direction of usage)		×
No. 3	Interrupt handling during self-programming mode (Specification change notice)		✓
No. 4	Subclock selection for WT, TAA, TMM (Specification change notice)		×
No. 5	TAA, TAB Anytime write delay (Direction of use)		×
No. 6	Code Flash and Data Flash operation (Specification Change Notice)		×

a. The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

Outline			μPD70F3379
		Rev.	
		Rank[a]	
No. 1	Boot Cluster Swapping (I) (Direction of usage)		✓
No. 2	Boot Cluster Swapping (II) (Direction of usage)		✓
No. 3	Interrupt handling during self-programming mode (Specification change notice)		✓
No. 4	Subclock selection for WT, TAA, TMM (Specification change notice)		×
No. 5	TAA, TAB Anytime write delay (Direction of use)		×
No. 6	Code Flash and Data Flash operation (Specification Change Notice)		×

a. The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

Outline			μPD70F3380
		Rev.	
		Rank[a]	
No. 1	Boot Cluster Swapping (I) (Direction of usage)		✓
No. 2	Boot Cluster Swapping (II) (Direction of usage)		✓
No. 3	Interrupt handling during self-programming mode (Specification change notice)		✓
No. 4	Subclock selection for WT, TAA, TMM (Specification change notice)		×
No. 5	TAA, TAB Anytime write delay (Direction of use)		×
No. 6	Code Flash and Data Flash operation (Specification Change Notice)		×

a. The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

Outline			μPD70F3381
		Rev.	
		Rank[a]	
No. 1	Boot Cluster Swapping (I) (Direction of usage)		✓
No. 2	Boot Cluster Swapping (II) (Direction of usage)		✓
No. 3	Interrupt handling during self-programming mode (Specification change notice)		✓
No. 4	Subclock selection for WT, TAA, TMM (Specification change notice)		×
No. 5	TAA, TAB Anytime write delay (Direction of use)		×
No. 6	Code Flash and Data Flash operation (Specification Change Notice)		×

a. The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

Outline			µPD70F3382
		Rev.	
		Rank[a]	
No. 1	Boot Cluster Swapping (I) (Direction of usage)		✓
No. 2	Boot Cluster Swapping (II) (Direction of usage)		✓
No. 3	Interrupt handling during self-programming mode (Specification change notice)		✓
No. 4	Subclock selection for WT, TAA, TMM (Specification change notice)		×
No. 5	TAA, TAB Anytime write delay (Direction of use)		×
No. 6	Code Flash and Data Flash operation (Specification Change Notice)		×

a. The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

✓: Not applicable
×: Applicable

V850ES/FK3

Outline			μPD70F3383
		Rev.	
		Rank[a]	
No. 1	Boot Cluster Swapping (I) (Direction of usage)		✓
No. 2	Boot Cluster Swapping (II) (Direction of usage)		✓
No. 3	Interrupt handling during self-programming mode (Specification change notice)		×
No. 4	Subclock selection for WT, TAA, TMM (Specification change notice)		×
No. 5	TAA, TAB Anytime write delay (Direction of use)		×
No. 6	Code Flash and Data Flash operation (Specification Change Notice)		×

a. The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

Outline			μPD70F3384
		Rev.	
		Rank[a]	
No. 1	Boot Cluster Swapping (I) (Direction of usage)		✓
No. 2	Boot Cluster Swapping (II) (Direction of usage)		✓
No. 3	Interrupt handling during self-programming mode (Specification change notice)		×
No. 4	Subclock selection for WT, TAA, TMM (Specification change notice)		×
No. 5	TAA, TAB Anytime write delay (Direction of use)		×
No. 6	Code Flash and Data Flash operation (Specification Change Notice)		×

a. The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

Outline			µPD70F3385
		Rev.	
		Rank[a]	
No. 1	Boot Cluster Swapping (I) (Direction of usage)		✓
No. 2	Boot Cluster Swapping (II) (Direction of usage)		✓
No. 3	Interrupt handling during self-programming mode (Specification change notice)		×
No. 4	Subclock selection for WT, TAA, TMM (Specification change notice)		×
No. 5	TAA, TAB Anytime write delay (Direction of use)		×
No. 6	Code Flash and Data Flash operation (Specification Change Notice)		×

a. The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

✓: Not applicable
×: Applicable

(B) Description of Operating Precautions

No. 1	Boot Cluster Swapping (I) (Direction of usage)

Details

When modifying the Code Flash while the boot cluster swapping is enabled use the single voltage flash self-programming library available V1.20 or later.
When executing on-chip debugging by connecting a NWIRE emulator use the EXEC.dll version V1.81 or later.

No. 2	Boot Cluster Swapping (II) (Direction of usage)

Details

On the PG-FP4 or PG-FP5 Flash Programmer before modifying the Code Flash while the boot cluster swapping is enabled issue the ChipErase-Command.

Read of data in swapped state will return the data in the unswapped stated, thus the addresses of data in the swapped area are wrong.

No. 3	Interrupt handling during self-programming mode (Specification change notice)

Details

When the device is in self-programming mode, the following interrupt handlers will not be executed and the related interrupts will not be serviced:

Name	Source	Handler address
INTUD6S	UARTD6 status interrupt	00000720H
INTUD7S	UARTD7 status interrupt	00000750H
INTAD1	A/D1 conversion completion	00000780H

Workaround

Do not use the above mentioned interrupts / -handlers in self-programming mode.

No. 4	Subclock selection for WT, TAA, TMM (Specification change notice)

Details

If both of the following conditions are met the f_{RL} (240 kHz internal oscillator) clock is selected as the input clock for a timer rather than the f_{XT} (subclock).

Conditions:

- The SUBCLK bit in the option byte at address 0x7B is set to 1 in order to select the f_{RL} (240 kHz internal oscillator) as clock source for the subclock operating mode.
- f_{XT} (subclock) is selected as the input clock for the Watchtimer (WT), Timer AA (TAA) or Timer M (TMM).

The above applies for the following timers in subclock operation mode:

- Watchtimer (WT),
- Timer AA (TAA) (only odd numbered macros of TAA are concerned if available on a specific device, e. g. TAAn, n = 1, 3, 5, 7),
- Timer M (TMM)

In other words: In subclock operation mode (i. e. subclock is selected as the CPU clock) the above mentioned timers (WT, TAA, TMM) are supplied by the same clock as the CPU (in this case f_{RL}) rather than by a fixed f_{XT} clock generated by the subclock oscillator.

No. 5 TAA, TAB Anytime write delay (Direction of use)

Details

This direction of use is applicable only for updating compare registers during timer operation with anytime write mechanism.
The time for the takeover of the new Compare value to the Compare register has to be taken into account regarding to the interrupt flag generation. The interrupt flag could be set during the delayed takeover of the compare value. This could happen, if the old compare value matches the timer counter. This will set the interrupt flag, even when the CPU already wrote a new value to the compare register.
TAAnCCRm and TABnCCRm register rewrite is possible during timer operation, but the write method (anytime write or reload) differs depending on the mode.
The anytime write method is only possible in following modes: Free-running mode, external event count mode, one-shot pulse mode and interval timer mode.
(PWM mode & external trigger pulse output mode use the reload mechanism).
Rewriting the value of the compare register is enabled during timer operation and a value can be written to the register at any time (when the value to be compared is written to the register, it is synchronized with the internal clock and compared with the value of the 16-bit counter).

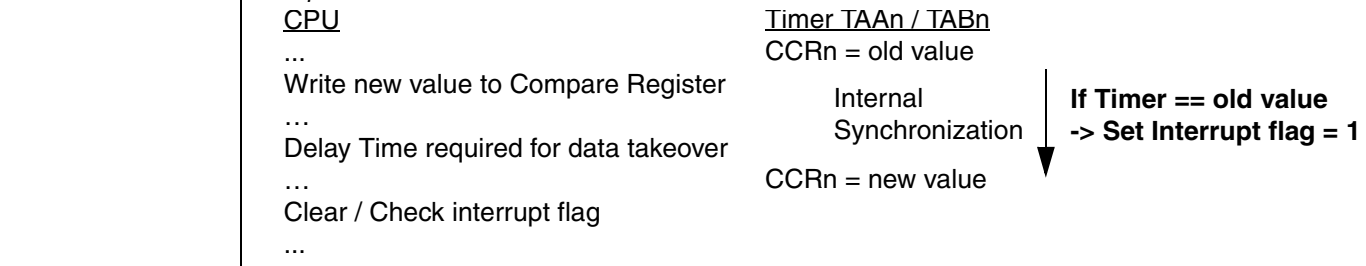
Depending on the application requirements, the possible interrupt flag generation after updating the compare register value, could influence the application operation.The time for updating the compare register has to be taken into account. If the interrupt should be reset by software, a certain delay after writing to the compare register has to be inserted.

The reason for the delayed takeover of the new compare register value is the timer's internal synchronisation and the different clock supply for the CPU and peripherals. The timers internal logic is clocked by the peripheral clock fxp1. The ralationship of CPU clock and clock fxp1 has to be included in the delay time calculation.

Conditions:

- Timer in Free-running mode, external event count mode, one-shot pulse mode or interval timer mode
- TAAnCCRm and TABnCCRm in compare mode
- Writing new compare value during timer operation
- Timer value equal to compare register value while updating the compare register

Example



Direction of use:

If the possible interrupt flag generation could influence the application operation, the following direction of use can avoid the interrupt flag generation.
The delay time for the compare register update should be allowed to pass before clearing or checking the interrupt flag.
The delay time depend on the peripheral clock setting for fxp1 (-> PRSI).
The delay time depend on the CPU clock setting for fcpu (-> PCC.3-0)
The delay time does NOT depend on the VSWC setting.
The delay time does NOT depend on the timer count clock (TAAnCKS2-0, TABnCKS2-0)

No. 5 TAA, TAB Anytime write delay (Direction of use)

There are two possible solutions for this purpose:

1. Writing twice to the compare register (same value, two times)
This is a simple solution to ensure a takeover before the CPU executes the next instruction. The CPU has to wait, because the peripheral will generate an active wait request. This solution always takes more time than required.
The advantage is a simple usage and short (additional 4 Bytes)implementation, but takes a few more CPU clock cycles than required.
(See User's Manual Appendix B for details of Register Access Times.)

2. Insert a minimum count of CPU clocks
A simple way to wait for a few CPU clocks, is to execute NOP instructions. It is also possible to replace the NOP instructions by any useful code before clearing/checking the interrupt flag.

Formula:
Required CPU clocks: 4 x fcpu / fxp1 + 3

Examples:
1. Writing the compare register twice
Valid for any possible CPU and peripheral clock configuration

```
st.h    r6, TAB1CCR2[r0]
st.h    r6, TAB1CCR2[r0]
clr1    7, TAB1CCIC2[r0]      // Clear interrupt flag TAB1CCIF2
...
```

2. Insert NOP instructions to ensure wait time
fxp1 = fxx/2 (PRSI=1), fcpu = fxx (PCC.3-0=0000b)

```
st.h    r7, TAA0CCR1[r0]      // Write new compare value
nop                           // 11 NOPs necessary ...
nop
nop
nop
nop
nop
nop
nop
nop
nop
nop
clr1    7, TAA0CCIC1[r0]      // Clear interrupt flag TAA0CCIF1
...
```

No. 6 Code Flash and Data Flash operation (Specification Change Notice)

Details

Before starting any operation (e.g. write, erase, verify) in Code or Data Flash, it is mandatory to ensure that no other operation beside read in either Code or Data Flash is in progress.

(C) Valid Specification

Item	Date published	Document No.	Comment
1	November 2007	U17793EE2V2UM00	V850ES/Fx3 Hardware (User's Manual)
2	April 2004	U15943EJ3V0UM00	V850ES Architecture (User's Manual)

(D) Revision History

Item	Date published	Document No.	Comment
1	November 2007	U19002EE1V0IF00	Initial release
2	April 2008	U19002EE1V1IF00	Added No. 3 for FK3 devices
3	April 2008	U19002EE1V2IF00	Added information for uPD70F3378, uPD70F3381, uPD70F3382
4	August 2008	U19002EE2V1IF00	Added No. 4.
5	April 2009	U19002EE2V2IF00	Added No. 5.
6	November 2009	U19002EE3V0IF00	Added No. 6.